HX9031A

Features

- **1.8V Single Supply**
- **Five sensor inputs**
- **Capacitance resolution up to 1aF**
- **Capacitance offset compensation up to 400pF**
- **Support fully differential input mode**
- **Smart SAR detection engine**
- **Advanced ambient environment compensation algorithm**
- **Programmable detection range**
- **Programmable scan period from 2ms to 4s**
- **Ultra-low EMI mode by enable spread spectrum**
- **Three level user proximity interrupts**
- **Low Power consumption**
  - Scan Mode: 25 uA
  - Doze Mode: 7 uA
  - Sleep Mode: 1 uA
- **Support up to 400kHz I2C Serial Interface**
- **Support 1.65~3.6V IO voltage**
- **Programmable Interrupt or Real-Time Status Pin**
- **Integrated temperature sense ADC for temperature compensation**
- **-40°C to +85°C Operation**
- **Compact Size: 1.8 x 2.1 mm LGA10**

Applications

Smart Phone, PAD, TWS
Head Phone, Smart Wearable

Description

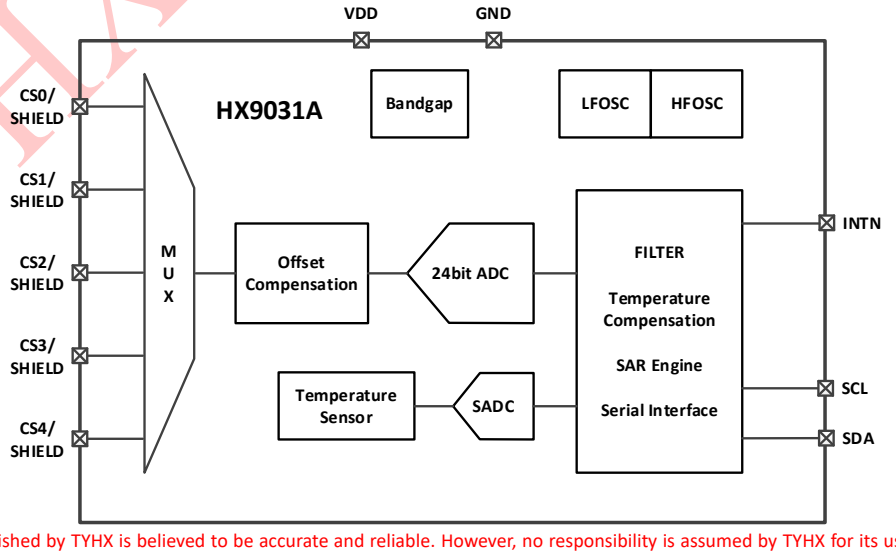
The HX9031A integrates a capacitance sense AFE used for Specific Absorption Rate (SAR) application.

The HX9031A supports up to five sensor inputs, with an offset compensation capacitance up to 400pF. The HX9031A has high sensitivity which enables the detection of human body proximity. The portable electronic device can reduce the emission power upon the presence of human body according to the detection result of HX9031A. This will bring significant performance advantages for manufacturers of electronic devices with electro-magnetic radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

The HX9031A can operate from 1.8V single supply, and it outputs data via I2C bus. The I2C serial communication bus port is compatible with 1.65~3.6V host control to report user proximity. Upon proximity detection, the INTN output asserts, enabling the user to either determine the relative proximity distance, or simply obtain an indication of detection.

HX9031A has on-chip calibration logic to account for changes in the ambient environment, such as temperature, humidity. The calibration sequence is performed automatically and at continuous intervals, while the sensors are not touched. This ensures that there are no false detections on the external sensors due to the changing environment.

Simplified Block Diagram



Contents

1 Pin Configuration

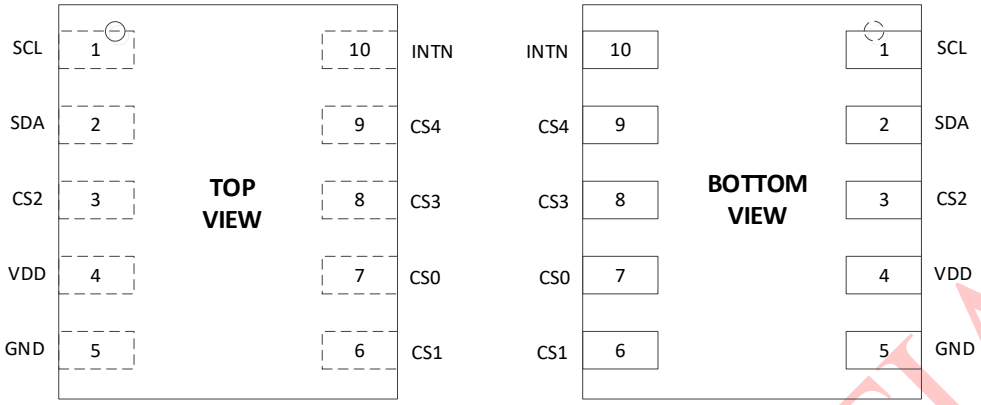


Figure1 HX9031A Pin Diagram

Table1 HX9031A Pin Description

Pin	Name	Type	Description
1	SCL	Digital	I2C CLK, external pull up resistor (recommended 2.2kΩ for 400KHz)
2	SDA	Digital	I2C data, external pull up resistor (recommended 2.2kΩ for 400KHz)
3	CS2	Analog	Capacitance Sensor Input
4	VDD	Power	Power Supply
5	GND	Ground	Power Ground
6	CS1	Analog	Capacitance Sensor Input
7	CS0	Analog	Capacitance Sensor Input
8	CS3	Analog	Capacitance Sensor Input
9	CS4	Analog	Capacitance Sensor Input
10	INTN	Digital	Interrupt output

2 Specifications

2.1 Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.5	2	V
Pull-up Voltage	VPULL	-0.5	3.6	V
Input Voltage(non-supply pins)	VIN	-0.5	VDD+0.3	V
Input Current(non-supply pins)	IIN	-10	10	mA
Operating Junction Temperature	TJCT	-40	125	℃
Reflow Temperature	TRE		260	℃
Storage Temperature	TSTOR	-50	150	℃

2.2 Recommended Operating Conditions

Parameter	Min	Max	Unit
VDD	1.65	1.98	V
Specified temperature range	-40	85	℃

2.3 ESD Ratings

Parameter		Value	Unit
V(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±500	

2.4 Electrical Characteristics

Typical specifications are at 25°C, VDD 1.8V, offset capacitor 30pF, OSR = 128, ODR = 5Hz, minimum and maximum specifications are at VDD = 1.64V to 1.98 V, Temp = −40°C to +85°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Conversion Rate	2	200	4000	ms	Programmable
Resolution	4		100	aF/LSB	Programmable
Input Range	±1.25		±10	pF	Programmable
Input Channel Linearity		±3		fF	
Sampling Frequency	4		800	kHz	
RMS Noise @30pF load		30		aF	
RMS Noise @200pF load		200		aF	
Input Leakage			1	nA	
Gain Error			3	%	
Offset Compensation Range			400	nF	
Offset Compensation Resolution		234.375		fF	
Input RC Resistor	400		4k	Ω	Programmable
Input RC Capacitor		5		pF	
Total Internal Channel Capacitance		6		pF	Total channel capacitance measured at the ball; guaranteed by design
Current Consumption					
Full Power		1.1		mA	1KHz conversation rate
Scan Mode		25		μA	OSR=128, Single channel, ODR=5Hz
Doze Mode		7		μA	OSR=128, Single channel, ODR=2.5Hz
Sleep Mode		1		uA	Sleep Mode
Inputs SCL,SDA					
Input High Voltage, VIH	0.7 × VIO			V	
Input Low Voltage, VIL			0.2 × VDD	V	
Input High Current, IIH	−1			μA	VIN = 1.8
Input Low Current, IIL			1	μA	VIN = 0V
Open-Drain Outputs (SDA, INTN)					
Output Low Voltage, VOL			+0.3 × VIO	V	ISINK = −3 mA
Output High Leakage Current, IOH		±0.1	±1	μA	VOUT = 1.8 V
INTERNAL OSCILLATOR					
HFOSC Frequency		5		MHz	
HFOSC Accuracy			±4	%	
LFOSC Frequency		32		kHz	

LFOSC Accuracy			±4	%	
POWER-ON RESET					
Power-Down Level			0.2	V	
Power-On Level	1.5			V	
VDD	1.65		1.98	V	

3 Detailed Description

3.1 Overview

The HX9031A integrates a capacitance sense AFE used for Specific Absorption Rate (SAR) application. The HX9031A supports up to five sensor inputs, with an offset compensation capacitance up to 400F. The HX9031A has high sensitivity which enables the detection of human body proximity. The portable electronic device can reduce the emission power upon the presence of human body according to the detection result of HX9031A. This will bring significant performance advantages for manufacturers of electronic devices with electro-magnetic radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

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3.2 Functional Block Diagram

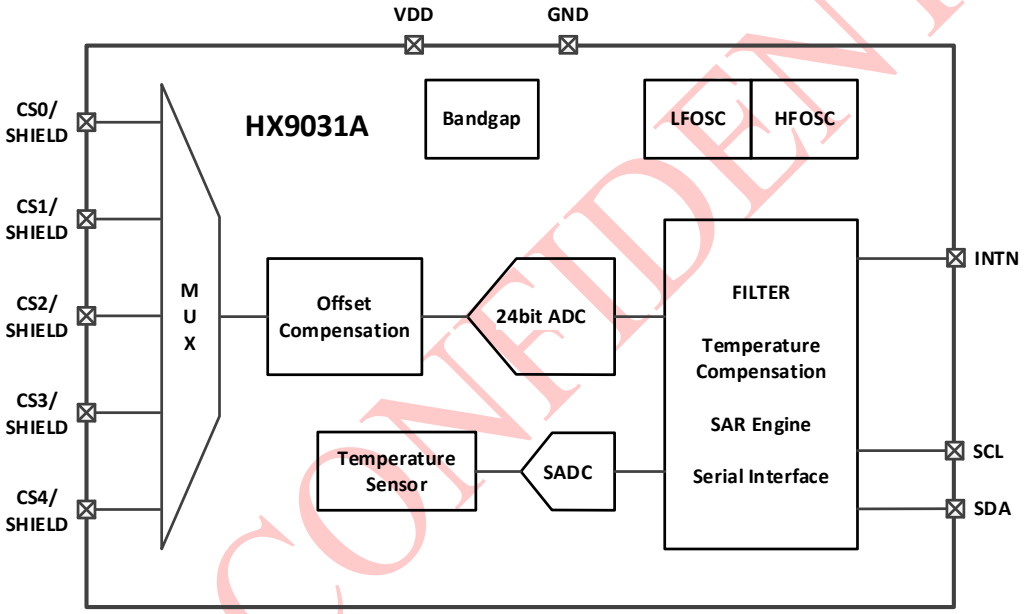


Figure2 Functional Block Diagram

3.3 Working Mode

HX9031A has mainly three operation modes

1 sleep mode: which is configured if no CH_EN is enabled. All the circuits except I2C and 32KHz OSC are shut down and the power consumption is less than 1uA.

2 scan mode: if any of the CH_NUM[3:0] is enabled, HX9031A will go to scan mode, in this mode the chip will periodically detect the capacitance on each sensor (if enabled). The scan period can be configured by register.

3 Doze mode: In some applications, the reaction/sensing time needs to be fast when the user is present (proximity detected), but can be slow when no detection has occurred for some time. If doze mode is enabled, the HX9031A will scan each channel (if enabled) by a relatively slow rate, and if user proximity is detected, it will accelerate the scan period and back to slow rate when proximity is released.

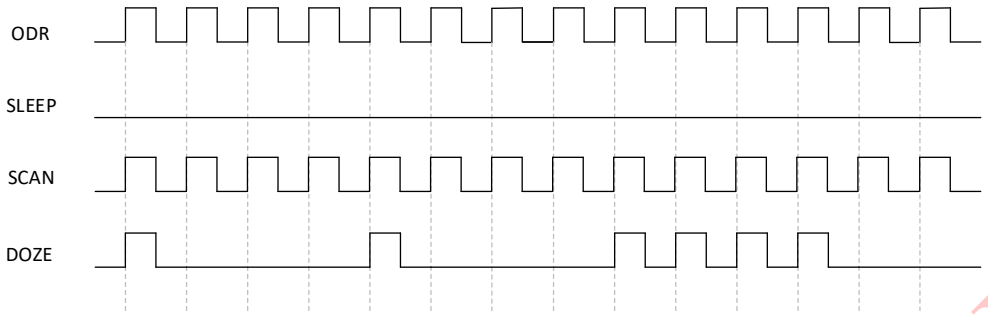


Figure3 Working modes of HX9031A

3.4 Timing Diagram

The timing information of HX9031A is as following. The device works under two internal clocks: 32KHz system clock CLK_32K and 5MHz ADC timing clock CLK_5M. The 32KHz clock is running all the time. It controls the scan period configured by register scan_period_i2c. The 5MHz high frequency clock is enabled in scan mode or doze mode. It is used to generate the timing during each conversion.

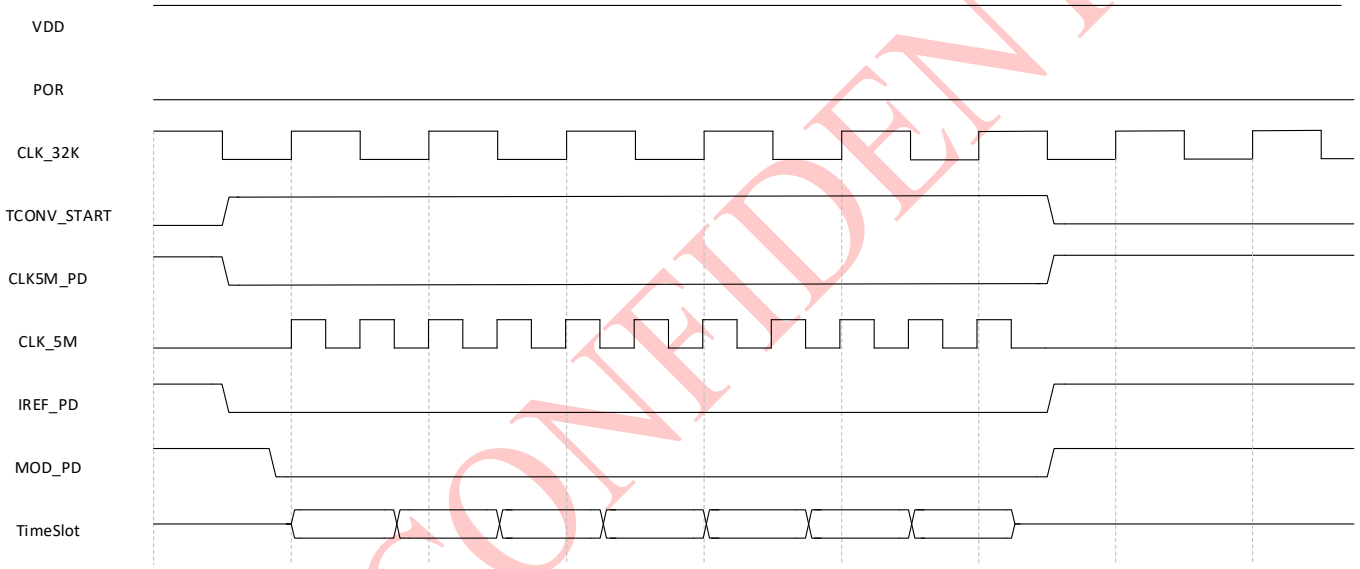


Figure4 Main Timing Diagram

3.5 Analog-to-Digital Converter (ADC)

A delta-sigma ADC is used to convert the input capacitance to a 16bit digital data. The ADC is highly configurable, user can configure the sample frequency, OSR, average time according the application.

The OSR and average number of each channel can be flexible configured through register. This can help the customer optimized the chip performance according different application environment.

Chx_avg_num_i2c: controls the average number of each channel. The down sample filter will output one data after averaged by NAVG times, this will improve the noise performance.

Chx_osr_num_i2c: controls the OSR of the ADC, the OSR can be configured as 64/128/256/512/1024, depending on the noise and resolution requirement.

Range_i2c: the full scale of the measurement can be configured separately for each channel. The full scale can be configured as 1.25pF/2.5pF/3.75pF/5pF depending on the application.

3.6 Offset Capacitance Compensation

The offset compensation scheme is used to compensate the capacitance of the sensor to the environment, i.e. PCB board. After the compensation, only the Cuser is feed into the ADC. HX9031A can compensate up to 40pF parasitic cap. The offset cap calibration will be performed before the first measurement and after the calibration, the offset value will be stored into register for each channel.

There are three sources that will trigger the compensation: 1. The compensation will be required when any of the channel is enabled. The compensation is performed before the first measurement. 2. The compensation can be trigger by the user writing a 1 to offset_cali_en_i2c. The offset calibration engine will start right before the next scan period. 3. The DSP will continuously

monitor the drift of the Cbulk, when the drift exceeds a certain level preset by the user, the offset calibration scheme will be performed.

The compensation request flag can be set anytime but the compensation scheme will be performed at the beginning of next scan period to keep all parameters coherent. Also, when compensation occurs, all the data in the low pass filter will be reset.

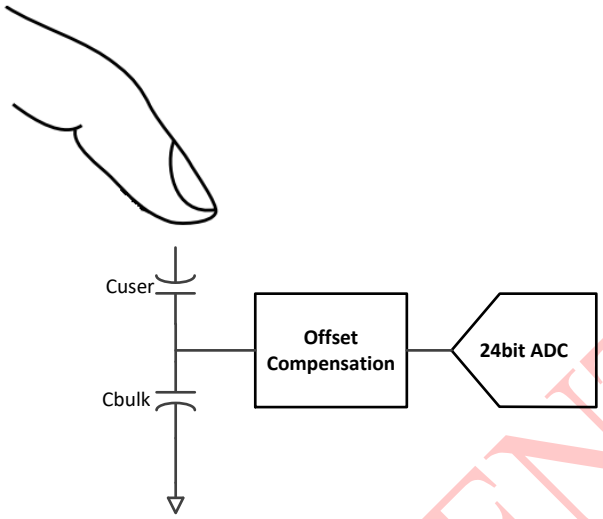


Figure5 Offset Compensation

3.7 Digital Signal Processing

The Digital Signal Processing (DSP) block is incorporated to convert the raw_data from the delta-sigma ADC to a low noise, environment robust prox_diff data which is used to indicate whether a proximity occurs. The offset calibration is performed once before the first measurement. But the environment will vary all the time, the Cbulk will drift along time. The DSP block will continuously monitor the environment drift and filter out the drift to get an environment insensitive prox_diff data.

Figure6 shows the digital processing sequence, after wake up, the digital will repeatedly update the raw_data, prox_diff, pros_stat of each channel.

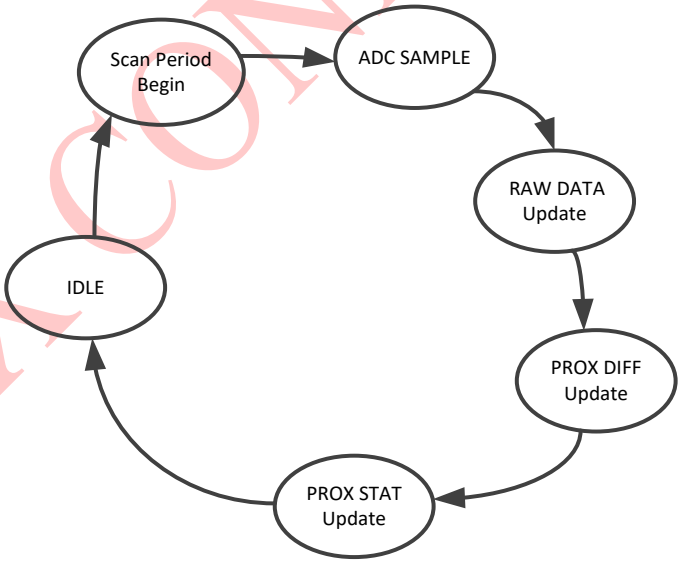


Figure6 Digital Processing Sequence

4 Register Map

Address	Name	R/W	BIT	Function	Default
0x00	GLOBAL_CTRL0	RW	<6>	enable spread spectrum function when set to 1	0x00
0x01	GLOBAL_CTRL1	RW	<7>	enable chop function when set to 1	0x02
0x02	PRF_CFG	RW	<4:0>	Defines the scan period 00000: Min (no idle time) 00001: 2ms 00010: 4ms 00011: 6ms 00100: 8ms 00101: 10ms 00110: 14ms 00111: 18ms 01000: 22ms 01001: 26ms 01010: 30ms 01011: 34ms 01100: 38ms 01101: 42ms 01110: 46ms 01111: 50ms 10000: 56ms 10001: 62ms 10010: 68ms 10011: 74ms 10100: 80ms 10101: 90ms 10110: 100ms 10111: 200ms default 11000: 300ms 11001: 400ms 11010: 600ms 11011: 800ms 11100: 1s	0x17
0x03	CH0_CFG_7_0	RW	<7:6>	Defines the connection of CS2 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
			<5:4>	Defines the connection of CS0 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11: Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11: Positive	
			<1:0>	Defines the connection of CS3 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11: Positive	
0x04	CH0_CFG_9_8	RW	<1:0>	Defines the connection of CS4 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
0x05	CH1_CFG_7_0	RW	<7:6>	Defines the connection of CS2 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
			<5:4>	Defines the connection of CS0 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11: Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11: Positive	
			<1:0>	Defines the connection of CS3 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11: Positive	
0x06	CH1_CFG_9_8	RW	<1:0>	Defines the connection of CS4 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
0x07	CH2_CFG_7_0	RW	<7:6>	Defines the connection of CS2 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
			<5:4>	Defines the connection of CS0 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11: Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11: Positive	
			<1:0>	Defines the connection of CS3 during conversion phase CH2	

				00: Non connected 01: Shield 10: Negative 11: Positive	
0x08	CH2_CFG_9_8	RW	<1:0>	Defines the connection of CS4 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
0x09	CH3_CFG_7_0	RW	<7:6>	Defines the connection of CS2 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
			<5:4>	Defines the connection of CS0 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11: Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11: Positive	
			<1:0>	Defines the connection of CS3 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11: Positive	
0x0a	CH3_CFG_9_8	RW	<1:0>	Defines the connection of CS4 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11: Positive	0x00
0x0D	RANGE_1_0	RW	<6:4>	Defines the full scale of conversion phase CH1 000: 1.25pF 001: 2.5pF 010: 3.75pF 011: 5pF 100: 0.625pF	0x00
			<2:0>	Defines the full scale of conversion phase CH0 000: 1.25pF 001: 2.5pF 010: 3.75pF 011: 5pF 100: 0.625pF	
0x0E	RANGE_3_2	RW	<6:4>	Defines the full scale of conversion phase CH3 000: 1.25pF 001: 2.5pF 010: 3.75pF 011: 5pF 100: 0.625pF	0x00
			<2:0>	Defines the full scale of conversion phase CH2 000: 1.25pF 001: 2.5pF 010: 3.75pF 011: 5pF 100: 0.625pF	
0x10	AVG0_NOSR0_CFG	RW	<7:5>	Defines the adc avg number of CH0 3'b000: data0_avg_num = 'd1 3'b001: data0_avg_num = 'd2 default 3'b010: data0_avg_num = 'd4 3'b011: data0_avg_num = 'd8 3'b100: data0_avg_num = 'd16 3'b101: data0_avg_num = 'd32	0x29
			<4:2>	Defines the adc OSR of CH0 3'b000: nosr_num = 'd16 3'b001: nosr_num = 'd32 3'b010: nosr_num = 'd64 default 3'b011: nosr_num = 'd128 3'b100: nosr_num = 'd256 3'b101: nosr_num = 'd512 3'b110: nosr_num = 'd1024	
			<1:0>	Reserved	
0x11	NOSR12_CFG	RW	<6:4>	Defines the adc OSR of CH2 3'b000: nosr_num = 'd16 3'b001: nosr_num = 'd32 3'b010: nosr_num = 'd64 default 3'b011: nosr_num = 'd128 3'b100: nosr_num = 'd256 3'b101: nosr_num = 'd512 3'b110: nosr_num = 'd1024	0x22
			<2:0>	Defines the adc OSR of CH1	

				3'b000: nosr_num = 'd16 3'b001: nosr_num = 'd32 3'b010: nosr_num = 'd64 default 3'b011: nosr_num = 'd128 3'b100: nosr_num = 'd256 3'b101: nosr_num = 'd512 3'b110: nosr_num = 'd1024	
0x12	NOSR43_CFG	RW	<2:0>	Defines the adc OSR of CH3 3'b000: nosr_num = 'd16 3'b001: nosr_num = 'd32 3'b010: nosr_num = 'd64 default 3'b011: nosr_num = 'd128 3'b100: nosr_num = 'd256 3'b101: nosr_num = 'd512	0x12
0x13	AVG12_CFG	RW	<6:4>	Defines the adc avg number of CH2 3'b000: data0_avg_num = 'd1 3'b001: data0_avg_num = 'd2 default 3'b010: data0_avg_num = 'd4 3'b011: data0_avg_num = 'd8 3'b100: data0_avg_num = 'd16 3'b101: data0_avg_num = 'd32	0x11
			<2:0>	Defines the adc avg number of CH1 3'b000: data0_avg_num = 'd1 3'b001: data0_avg_num = 'd2 default 3'b010: data0_avg_num = 'd4 3'b011: data0_avg_num = 'd8 3'b100: data0_avg_num = 'd16 3'b101: data0_avg_num = 'd32	
0x14	AVG34_CFG	RW	<2:0>	Defines the adc avg number of CH1 3'b000: data0_avg_num = 'd1 3'b001: data0_avg_num = 'd2 default 3'b010: data0_avg_num = 'd4 3'b011: data0_avg_num = 'd8 3'b100: data0_avg_num = 'd16 3'b101: data0_avg_num = 'd32	0x01
0x15	OFFSET_DAC0_7_0	RW	<7:0>	Defines the offset capacitance during CH0 001: 58.6 ff 002: 117.2 ff … … 100: 15pF … … FFF: 240pF	0x00
0x16	OFFSET_DAC0_11_8	RW	<3:0>		0x00
0x17	OFFSET_DAC1_7_0	RW	<7:0>	Defines the offset capacitance during CH1 001: 58.6 ff 002: 117.2 ff … … 100: 15pF … … FFF: 240pF	0x00
0x18	OFFSET_DAC1_11_8	RW	<3:0>		0x00
0x19	OFFSET_DAC2_7_0	RW	<7:0>	Defines the offset capacitance during CH2 001: 58.6 ff 002: 117.2 ff … … 100: 15pF … … FFF: 240pF	0x00
0x1A	OFFSET_DAC2_11_8	RW	<3:0>		0x00
0x1B	OFFSET_DAC3_7_0	RW	<7:0>	Defines the offset capacitance during CH3 001: 58.6 ff 002: 117.2 ff … … 100: 15pF … … FFF: 240pF	0x00
0x1C	OFFSET_DAC3_11_8	RW	<3:0>		0x00

0x1F	SAMPLE_NUM_7_0	RW	<7:0>	The 10bit register defines the sample frequency of the ADC, the sample frequency can be depicted with below formula: *Fsample = 1.0 / (sample_num * 200ns)*, while the sample_num is the value the register in decimal.	0x32
0x20	SAMPLE_NUM_9_8	RW	<1:0>		
0x21	INTEGRATION_NUM_7_0	RW	<7:0>	The integration num should be the same with the SAMPLE_NUM.	0x32
0x22	INTEGRATION_NUM_9_8	RW	<1:0>		
0x24	CH_NUM_CFG	RW	<3:0>	This register defines the phase en signal of [CH3, CH2, CH1, CH0], the corresponding conversion phase will be started when set to 1.	0x00
0x2A	LP_ALPHA_1_0_CFG	RW	<6:4>	Defines the coefficient of the first order low pass filter during CH1. 000: 1 001: 1/2(default) 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	0x01
			<2:0>	Defines the coefficient of the first order low pass filter during CH0. 000: 1 001: 1/2(default) 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	
0x2B	LP_ALPHA_3_2_CFG	RW	<6:4>	Defines the coefficient of the first order low pass filter during CH3. 000: 1 001: 1/2(default) 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	0x11
			<2:0>	Defines the coefficient of the first order low pass filter during CH2. 000: 1 001: 1/2(default) 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	
0x2C	UP_ALPHA_1_0_CFG	RW	<7:4>	Defines the up coefficient of the first order low pass filter during CH1. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256 1010: 1/512	0x88
			<3:0>	Defines the up coefficient of the first order low pass filter during CH0. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256	

				1010: 1/512	
0x2D	UP_ALPHA_3_2_CFG	RW	<7:4>	Defines the up coefficient of the first order low pass filter during CH3. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256 1010: 1/512	0x88
			<3:0>	Defines the up coefficient of the first order low pass filter during CH2. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256 1010: 1/512	
0x2E	DN_ALPHA_0_CFG	RW	<3:0>	Defines the down coefficient of the first order low pass filter during CH0. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256 1010: 1/512	0x10
0x2F	DN_ALPHA_2_1_CFG	RW	<7:4>	Defines the down coefficient of the first order low pass filter during CH2. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256 1010: 1/512	0x11
			<3:0>	Defines the down coefficient of the first order low pass filter during CH1. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256	

				1010: 1/512	
0x30	DN_ALPHA_4_3_CFG	RW	<3:0>	Defines the down coefficient of the first order low pass filter during CH3. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 default 1001: 1/256 1010: 1/512	0x01
0x31	RA_INT_CAP_CFG	RW	<7:4>	This register defines the shielding en signal of [CH3, CH2, CH1, CH0], the shielding function will be enabled when the corresponding bit is set to 1.	0x00
0x38	RA_RAW_BL_RD_CFG	RW	<7:4>	Defines the output data of [CH3 CH2 CH1 CH0], the output data is raw_data when set to 0, and bl_data when set to 1	0xff
			<3:0>	Defines the output data of [CH3 CH2 CH1 CH0], the output data is lp_data when set to 0, and diff_data when set to 1	
0x39	INTERRUPT_CFG	RW	<7:4>	Enable the interrupt function of [CH3 CH2 CH1 CH0] when proximity occurs	0xff
			<3:0>	Enable the interrupt function of [CH3 CH2 CH1 CH0] when proximity releases	
0x3B	CALI_THRES_CFG	RW	<7:4>	Enable the interrupt function of [CH3 CH2 CH1 CH0] when the conversion is ready	0x07
			<3:0>	Defines the threshold of the offset compensation, when abs(bl_data) exceeds the threshold, the conversion phase will be compensated again. 0000: 2048 0001: 4096 … … 0111: 16384 default … … 1111: 32768	
0x3C	DITHER_CFG	RW	<2>	Define the shape of the dither 0: rectangle 1: triangle	0x21
			<1:0>	Defines the dither strength 0: 1/8 1: 1/4 2: 1/2 3: 1	
0x60	DEVICE_ID	RO	<7:0>	DEVICE ID	0x1D
0x62	TEMP_DATA_7_0	RO	<7:0>	The 10bit register is the output data of the temperature sense ADC, it's un-signed 10bit code	0x00
0x63	TEMP_DATA_9_8	RO	<1:0>		0x00
0x6B	PROX_STATUS	RO	<3:0>	Indicates the proximity occurrence of [CH3 CH2 CH1 CH0]	0x00
0x6C	PROX_INT_HIGH_CFG	RW	<3:0>	Defines the Proximity persistency number(Near) 0001: 1 0010: 2 0011: 3 … … 1110: 14 1111: 15	0x01
0x6D	PROX_INT_LOW_CFG	RW	<3:0>	Defines the Proximity persistency number(Far) 0001: 1 0010: 2 0011: 3 … … 1110: 14 1111: 15	0x01
0x6F	INT_WIDTH_7_0	RW	<7:0>	The 9bit code defines the Interrupt pulse width, and the formula is Int_width*32us	0x1F
0x70	INT_WIDTH_8	RW	<0>		0x00

0x71	INT_STATE_RD0	RO	<7:0>	Interrupt status reg0 [0]: CH0 far status [1]: CH1 far status [2]: CH2 far status [3]: CH3 far status [4]: CH0 near status [5]: CH1 near status [6]: CH2 near status [7]: CH3 near status	0x00
0x72	INT_STATE_RD1	RO	<7:4>	[4]: Offset compensation is triggered in CH0 [5]: Offset compensation is triggered in CH1 [6]: Offset compensation is triggered in CH2 [7]: Offset compensation is triggered in CH3	0x00
0x80	PROX_HIGH_THRES_CFG0_0	RW	<7:0>	Defines the CH0 proximity high threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x40
0x81	PROX_HIGH_THRES_CFG0_1	RW	<1:0>		0x00
0x82	PROX_HIGH_THRES_CFG1_0	RW	<7:0>	Defines the CH1 proximity high threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x40
0x83	PROX_HIGH_THRES_CFG1_1	RW	<1:0>		0x00
0x84	PROX_HIGH_THRES_CFG2_0	RW	<7:0>	Defines the CH2 proximity high threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x40
0x85	PROX_HIGH_THRES_CFG2_1	RW	<1:0>		0x00
0x86	PROX_HIGH_THRES_CFG3_0	RW	<7:0>	Defines the CH3 proximity high threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x40
0x87	PROX_HIGH_THRES_CFG3_1	RW	<1:0>		0x00
0x88	PROX_LOW_THRES_CFG0_0	RW	<7:0>	Defines the CH0 proximity low threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x20
0x89	PROX_LOW_THRES_CFG0_1	RW	<1:0>		0x00
0x8A	PROX_LOW_THRES_CFG1_0	RW	<7:0>	Defines the CH1 proximity low threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x20
0x8B	PROX_LOW_THRES_CFG1_1	RW	<1:0>		0x00
0x8C	PROX_LOW_THRES_CFG2_0	RW	<7:0>	Defines the CH2 proximity low threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x20
0x8D	PROX_LOW_THRES_CFG2_1	RW	<1:0>		0x00

0x8E	PROX_LOW_THRES_CFG3_0	RW	<7:0>	Defines the CH3 proximity low threshold 0x001: 32 0x002: 64 … … 0x100: 8192 … … 0x3FF: 32736	0x20
0x8F	PROX_LOW_THRES_CFG3_1	RW	<1:0>		0x00
0xe8	RA_RAW_BL_CH0_0	RO	<7:0>	CH0 raw_data or baseline data, bit 7:0	0x00
0xe9	RA_RAW_BL_CH0_1	RO	<7:0>	CH0 raw_data or baseline data, bit 15:8	0x00
0xea	RA_RAW_BL_CH0_2	RO	<7:0>	CH0 raw_data or baseline data, bit 23:16	0x00
0xeb	RA_RAW_BL_CH1_0	RO	<7:0>	CH1 raw_data or baseline data, bit 7:0	0x00
0xec	RA_RAW_BL_CH1_1	RO	<7:0>	CH1 raw_data or baseline data, bit 15:8	0x00
0xed	RA_RAW_BL_CH1_2	RO	<7:0>	CH1 raw_data or baseline data, bit 23:16	0x00
0xee	RA_RAW_BL_CH2_0	RO	<7:0>	CH2 raw_data or baseline data, bit 7:0	0x00
0xef	RA_RAW_BL_CH2_1	RO	<7:0>	CH2 raw_data or baseline data, bit 15:8	0x00
0xf0	RA_RAW_BL_CH2_2	RO	<7:0>	CH2 raw_data or baseline data, bit 23:16	0x00
0xf1	RA_RAW_BL_CH3_0	RO	<7:0>	CH3 raw_data or baseline data, bit 7:0	0x00
0xf2	RA_RAW_BL_CH3_1	RO	<7:0>	CH3 raw_data or baseline data, bit 15:8	0x00
0xf3	RA_RAW_BL_CH3_2	RO	<7:0>	CH3 raw_data or baseline data, bit 23:16	0x00
0xf4	RA_LP_DIFF_CH0_0	RO	<7:0>	CH0 lp_data or diff data, bit 7:0	0x00
0xf5	RA_LP_DIFF_CH0_1	RO	<7:0>	CH0 lp_data or diff data, bit 15:8	0x00
0xf6	RA_LP_DIFF_CH0_2	RO	<7:0>	CH0 lp_data or diff data, bit 23:16	0x00
0xf7	RA_LP_DIFF_CH1_0	RO	<7:0>	CH1 lp_data or diff data, bit 7:0	0x00
0xf8	RA_LP_DIFF_CH1_1	RO	<7:0>	CH1 lp_data or diff data, bit 15:8	0x00
0xf9	RA_LP_DIFF_CH1_2	RO	<7:0>	CH1 lp_data or diff data, bit 23:16	0x00
0xfa	RA_LP_DIFF_CH2_0	RO	<7:0>	CH2 lp_data or diff data, bit 7:0	0x00
0xfb	RA_LP_DIFF_CH2_1	RO	<7:0>	CH2 lp_data or diff data, bit 15:8	0x00
0xfc	RA_LP_DIFF_CH2_2	RO	<7:0>	CH2 lp_data or diff data, bit 23:16	0x00
0xfd	RA_LP_DIFF_CH3_0	RO	<7:0>	CH3 lp_data or diff data, bit 7:0	0x00
0xfe	RA_LP_DIFF_CH3_1	RO	<7:0>	CH3 lp_data or diff data, bit 15:8	0x00
0xff	RA_LP_DIFF_CH3_2	RO	<7:0>	CH3 lp_data or diff data, bit 23:16	0x00

5 I2C Protocol

5.1 I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device address is 0x28. The register index will automatically increase by 1 after the addressed register has been accessed (read or write). And the format is shown as following:

A Acknowledge (0)

P Stop Condition

R Read (1)

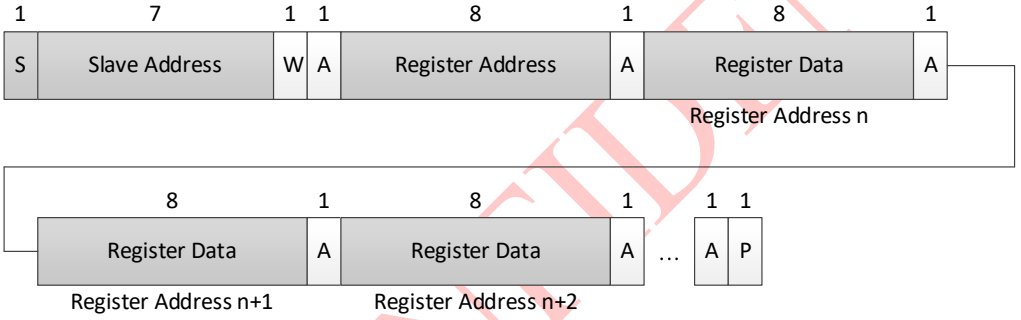
S Start Condition

W Write (0)

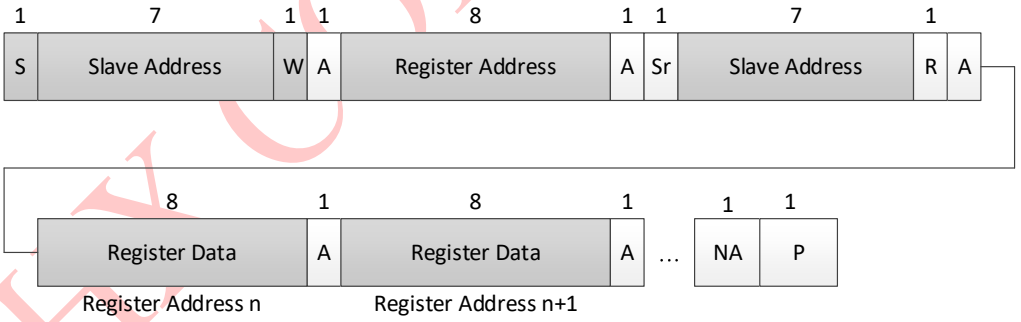
Sr Repeated Start Condition

■Master-to- Slave

□ Slave-to-Master



I2C Write Register Data



I2C Read Register Data

Figure7 I2C data format diagram

5.2 I2C Electrical Characteristics

Table2 I²C Electrical Characteristics

PARAMETER	SYMBOL	STANDARD		FAST		UNIT
		MIN	MAX	MIN	MAX	
LOW level input voltage: fixed input levels VDD-related input levels	VIL	 0.5 0.5	 1.5 0.3VDD	 n/a 0.5	 n/a 0.3VDD(1)	 V V
HIGH level input voltage: fixed input levels VDD-related input levels	VIH	 3 0.7VDD	 Note(2) Note(2)	 3 0.7VDD(1)	 n/a Note(2)	 V V
Hysteresis of Schmitt trigger inputs: VDD > 2 V VDD < 2 V	Vhys	 n/a n/a	 n/a n/a	 0.05VDD 0.1VDD	 – –	 V V

LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2 V VDD < 2 V	 VOL1 VOL2	 0 n/a	 0.4 n/a	 0 0	 0.4 0.2VDD	 V V
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	tof	–	250(4)	20+0.1 Cb(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1VDD and 0.9VDDmax	Ii	-10	10	-10(5)	10(5)	A
Capacitance for each I/O pin	Ci	-	10	-	10	pF

Notes

1. Devices that use non-standard supply voltage switch don't conform to the intended I2C-bus system levels must relate input levels to the VDD voltage to which the pull-up resistors Rp are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5V$.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table10.3.1(300ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

n/a = not applicable

5.3 I2C Timing

The I2C Timing is as following figure:

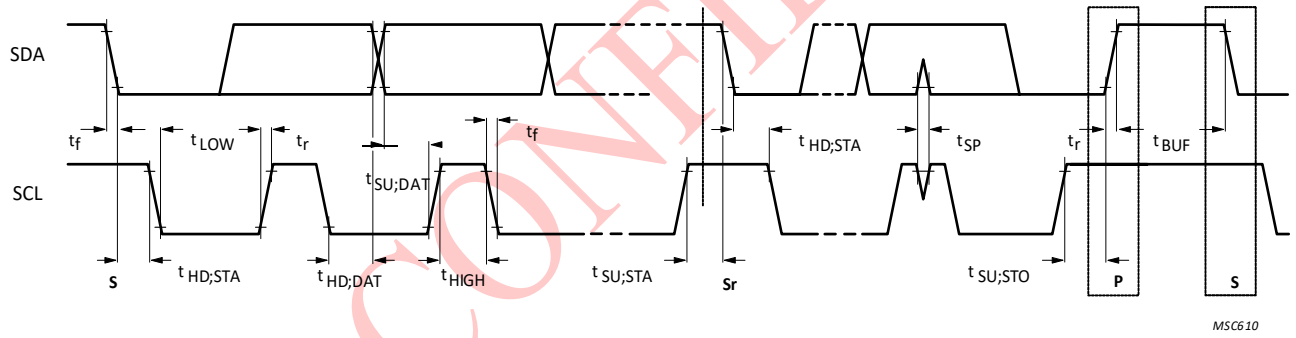


Figure8 I²C Timing

Table3 I²C Timing Parameters(1)

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL clock frequency	f_{SCL}	0	800	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	–	us
LOW period of the SCL clock	t_{LOW}	1.3	–	us
HIGH period of the SCL clock	t_{HIGH}	0.6	–	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	us
Data hold time	tHD;DAT	0(2)	–	us
Data set-up time	$t_{SU;DAT}$	100(3)	–	ns
Rise time of both SDA and SCL signals	tr	–	300	ns
Fall time of both SDA and SCL signals	tf	–	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	us
Capacitive load for each bus line	C_b	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1VDD	–	V

Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	V

Notes

1. All values referred to VIHmin and VILmax levels (see Table2).
2. A device must internally provide a hold time of at least 300ns for the SDA signal(referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU; DAT≥250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

6 Application Information

Typical application for HX9031A is showing below:

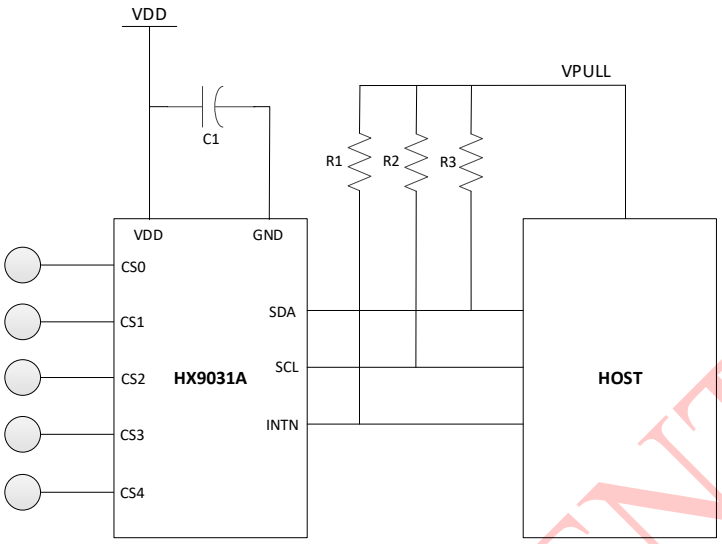


Figure9 Typical Application Schematic

Note:

1. Any CSx pad can be configured as dummy pad and at most five independent channels can be used simultaneously

And the device value is listed below:

Table4 I^2C Timing Parameters

DEVICE NAME	Value	Description
VDD	1.8V	Low noise
VPULL	1.65~3.6V	
C1	1uF	
R1	2.2 KΩ	
R2	2.2 KΩ	
R3	2.2 KΩ	

7 Package and Reel Information

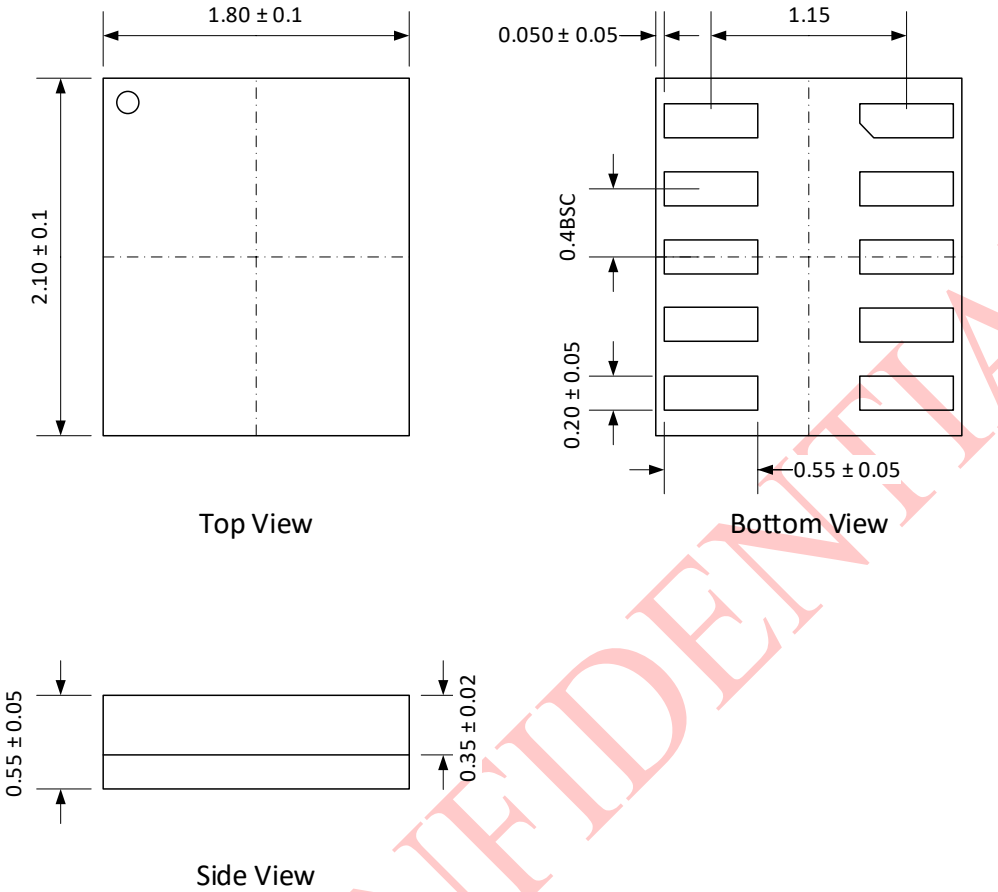


Figure10 Package Information (Unit: mm)

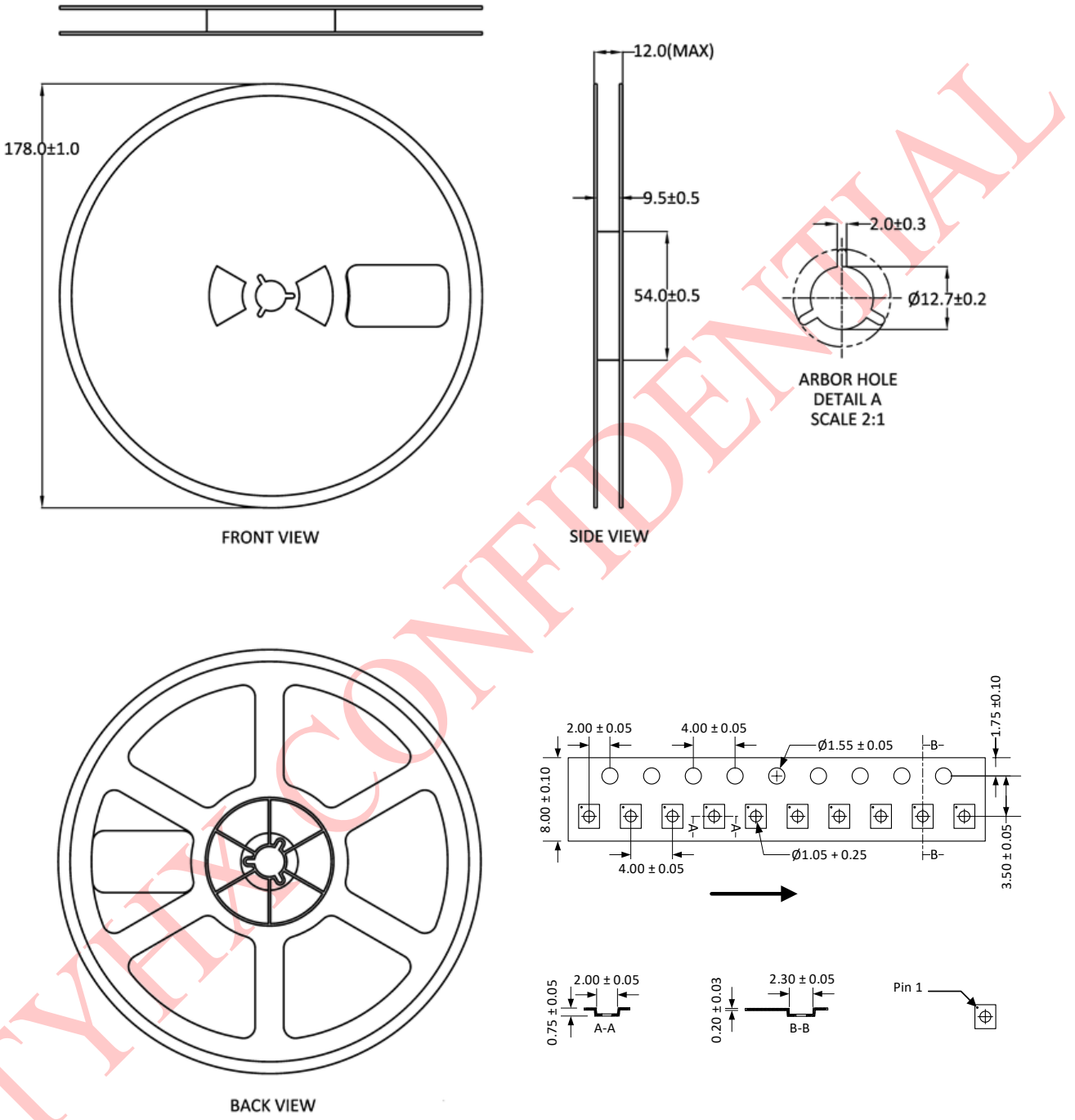


Figure11 Reel Information (Unit: mm)

7.1 Land Pattern

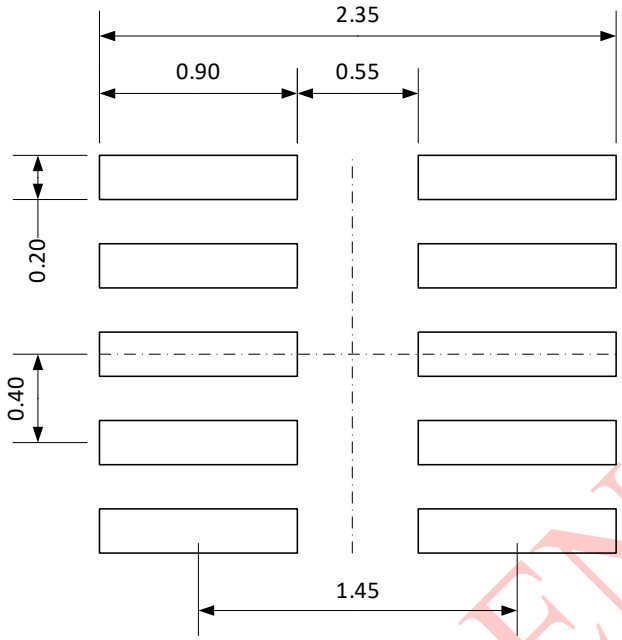


Figure12 Land Pattern

NOTES:

1. Controlling dimensions are in millimeters(angles in degrees).
2. This land pattern is for reference group to ensure your company's manufacturings are met.

8 Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and material used in these tests are detailed below. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

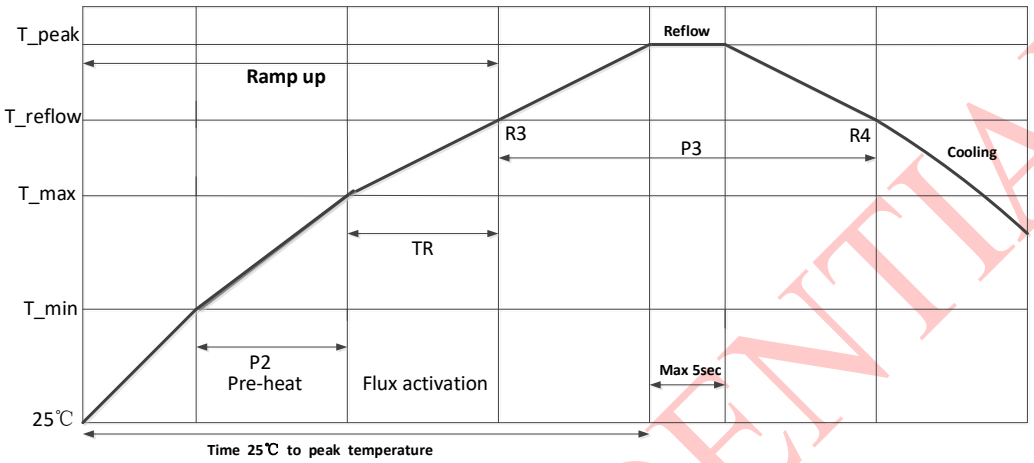


Figure13 Solder reflow profile grape

Table5 Solder Reflow Profile

	Peak temperature (Tpeak)	250-255℃; Max 5sec
Pre-Heat	Temperature min (Tmin)	150℃; 2℃/Sec
	Temperature max(Tmax)	150-217℃； 100S to 180S
	P2：（T min to max）	90-110s
Time maintain above	Temperature (Tre flow)	217℃
	Time (P3)	60-90sec
	R3 Slope (from 217℃ to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	480s Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

REVISION HISTORY

Version	Date	Comment
1.0	May 13, 2019	Initial version